

# High Power Density Thermoelectric Systems

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## Abstract

Broad usage of thermoelectric systems for high-wattage applications such as air conditioning and vehicle waste power recovery require much lower cost per unit of output than is presently achieved. Higher ZT materials and advanced thermodynamic cycles offer the promise of acceptable efficiency, but the cost and volume of such systems have remained unresolved limitations.

An approach is presented to reconfigure thermoelectric systems, which reduces bulk material usage and system size. The governing equations are presented and their application to advanced cycles that employ thermal isolation are discussed. Requirements and limitations to high power density operation are analyzed in terms of material and system properties. High power density configurations that maintain high thermodynamic efficiency are presented for operation with air, liquid, and solid working media. It is concluded that a factor of 10 to 25 reduction in thermoelectric material usage is possible for many important high-wattage applications.

## Background

The prospect of materials with a ZT substantially greater than unity has heightened interest in exploring applications of solid-state cooling/heating systems to replace conventional air-conditioners and other temperature control systems based on two phase compression cycles. The combination of material improvements with advanced thermodynamic cycles appear capable of addressing the performance deficiencies that have hampered implementation in the past. Several studies and discussions in the literature have described the performance and cost criteria for TE-based systems to be competitive [ 1, 2]. The criteria indicate that the cost of solid-state systems remains the final basic barrier to utilization of the new technology. Conventional TE modules are deficient both in the amount, and thus, cost, of TE material required to produce the several kilowatts of thermal cooling power required of typical air conditioning systems and the mechanical complexity of the heat transfer systems that thermally connect TE modules to air or other working fluids. New designs have been explored to address the high cost and complexity of such TE systems. To achieve the objective, the focus has been to (1) reduce substantially TE material usage, (2) develop configurations compatible with improved thermodynamic cycles and (3) simplify and reduce parasitic thermal and electrical system losses. The goal has been to reduce substantially the cost per watt of delivered thermal power while maintaining efficiency improvements associated with advanced cycles and higher ZT materials.

It is well known that the basic idealized equations for coefficient of performance (COP) and thermal cooling power,  $Q_C$ , are not associated with a scaling dimension, and thus, the value of COP and  $Q_C$  do not depend on physical size, but only

on intrinsic material properties and the length/area (L/A) ratios of TE elements. Performance of actual devices will change with size because of several non-ideal loss mechanisms that are addressed later in this paper, but to a first order, performance is independent of size if the L/A ratio is held constant.

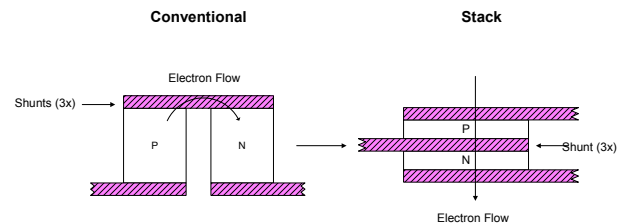
The question becomes, is the amount TE material used in today's modules as small as practical to offer the lowest cost per watt of cooling, or, are further reductions possible? If so, how much reduction can be achieved? While many factors contribute to parasitic losses, three tend to dominate in typical applications:

1. **Shunt Electrical Resistance.** The ohmic resistance of shunts connecting adjacent TE elements.
2. **Interfacial Metallic/Semiconductor Electrical Resistance.** The non-ohmic resistance associated with the depletion layer at the TE material/shunt interface.
3. **Heat Exchanger Thermal Resistance.** Temperature differentials associated with heat transport and heat exchanger losses external to the hot and cold interfaces of the TE elements.

The relationship between these parasitic losses and the amount of TE material used is analyzed in this paper to determine what practical reduction is possible.

## Analysis

Alternatives to standard module design can be beneficial in reducing shunt electrical resistance, and also providing options to address thermal heat exchange resistance. Figure 1 shows the conventional design to the left and a preferred alternative to the right.



**Figure 1:** Conventional and stack configurations.

This preferred design has the added advantage that it is ideally compatible with the thermal isolation techniques that enhance TE system thermodynamic efficiency, as described previously by the author [3]. Although other geometries are possible that reduce parasitic losses, in this paper the geometry on the right in Figure 1 will be used. The geometry, called a stack design, has been discussed previously for some applications by Berthet and by Stockholm [4, 5], but not for the specific purpose of minimizing the required amount of TE material.

The shunt resistance for the conventional geometry is given approximately by;

$$(1) \quad R_C = \frac{\rho_C L_C}{A_C}$$

and, correspondingly, for the stack;

$$(2) \quad R_S = \frac{\rho_S L_S}{A_S}$$

The ratio of the resistances, for the dimensions defined in Figure 2 is;

$$(3) \quad \frac{R_S}{R_C} = \left( \frac{\rho_S}{\rho_C} \right) \left( \frac{L_S}{L_C} \right) \left( \frac{A_C}{A_S} \right)$$

$$(4) \quad \approx \left( \frac{\rho_S}{\rho_C} \right) \left( \frac{T_S}{G_C + Y_C} \right) \left( \frac{T_C X_C}{W_S Y_S} \right)$$

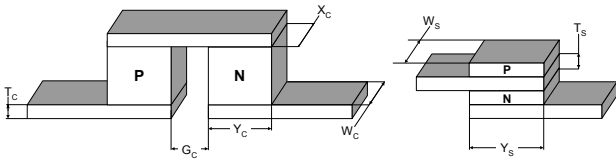
Typical values of the relevant dimensions are,

$$\begin{aligned} G_C &= 2.0\text{mm} & W_S &= 1.6\text{mm} \\ T_C &= 0.25\text{ mm} & X_C &= 2.4\text{mm} \\ T_S &= 2.5\text{mm} & Y_C &= Y_S = 1.6\text{mm} \\ \rho_S &= \rho_C \end{aligned}$$

Using these values;

$$(5) \quad \frac{R_S}{R_C} \approx 0.16$$

The ratio of about 0.16 provides sufficient parasitic resistance reduction to make the stack geometry very favorable for the purpose of reducing TE material usage, as will be discussed later.



**Figure 2:** Dimensional nomenclature of conventional and stack designs.

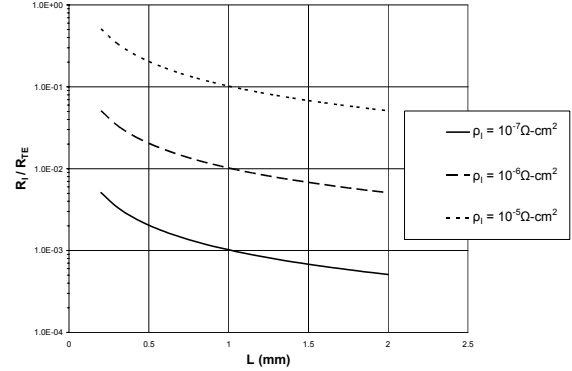
The second major source of loss is interfacial resistance between the metallic shunt and the TE semiconductor. The primary mechanism for interfacial resistance is the low carrier concentration in the depletion layer formed at such interfaces. This narrow region (about 1nm) is of high intrinsic resistivity. The resistance across the interface typically ranges from  $10^{-5}$  to  $10^{-8}\Omega\text{-cm}^2$ . The higher value is associated with simple plated contacts and the lower values with treatments that appropriately shorten the depletion layer thickness by increased carrier concentration (e.g. doping) in the depletion regions. The material systems employed should be designed to not degrade thermoelectric properties (i.e.,  $Z$ ) significantly near the interfaces.

The interfacial resistance,  $R_I$ , will be the same for conventional and stack configurations. It is necessary to understand the impact of interfacial resistance on system performance to determine the required resistance value for the stack design that will enable a meaningful reduction in material usage.

The ratio  $R_I/R_{TE}$  is;

$$(6) \quad \frac{R_I}{R_{TE}} = \frac{\frac{\rho_I}{A}}{\frac{\rho_{TE} L}{A}} = \frac{\rho_I}{\rho_{TE} L}$$

Thus, as  $L$  decreases, the ratio increases. Typical values for  $R_I/R_{TE}$  as a function of  $L$  for several values of  $\rho_I$  are given in Figure 3.



**Figure 3:** Interface/TE resistance ratio as a function of TE length.

A practical threshold for this resistance ratio is 0.01 to keep losses from degrading performance significantly. For example, this requires an interfacial resistance of about  $2 \times 10^{-7}\Omega\text{-cm}^2$  if  $L$  is about 0.3mm.

The impact of reducing parasitic resistances has been treated analytically as a lumped parameter by Parrott & Penn [6]. This analysis follows their approach. The impacts on TE performance of  $R_S$  and  $R_I$  are essentially equivalent and can be analyzed together. The net effect is to reduce  $Z_O$  by;

$$(7) \quad Z_L = \frac{Z_O}{(1 + \beta)}$$

where;

$$(8) \quad \beta = \frac{R_S}{R_{TE}} + \frac{R_I}{R_{TE}}$$

and;

$$(9) \quad Z_O = \frac{\alpha^2}{K_{TE} R_{TE}}$$

At maximum efficiency,  $COP_{OPT}$ , the cooling power,  $Q_{COPT}$ , the power input,  $Q_{INOPT}$ , optimum current,  $I_{OPT}$  and  $COP_{OPT}$  become;

$$(10) \quad I_{OPT} = \frac{\alpha}{R_{TE} (1 + \beta)} \frac{\Delta T}{(M_L - 1)}$$

$$(11) \quad Q_{COPT} = I_{OPT} \alpha T_C - \frac{1}{2} I_{OPT}^2 R_{TE} (1 + \beta) - K_{TE} \Delta T$$

$$(12) \quad Q_{INOPT} = I_{OPT} \alpha \Delta T + I_{OPT}^2 R_{TE} (1 + \beta)$$

$$(13) \quad COP_{OPT} = \frac{T_C}{\Delta T} \left( \frac{M_L - 1 - \frac{\Delta T}{T_C}}{M_L + 1} \right)$$

where;

$$(14) \quad M_L = \sqrt{1 + Z_L T_{AVE}}$$

The intention is to reduce the volume of TE material required to achieve the required cooling capacity at or near optimum efficiency. Written in terms of  $Z_O$  and  $L$ ;

$$(15) \quad \frac{Q_{COPT}}{AL} = \frac{K_{TE} \Delta T}{AL} \left( \frac{Z_L T_C}{(M_L - 1)} - \frac{Z_L \Delta T}{2(M_L - 1)^2} - 1 \right)$$

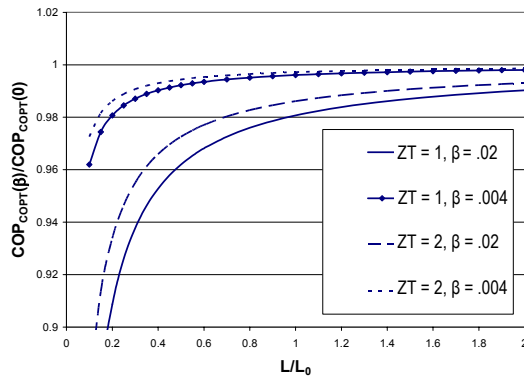
$$(16) \quad = \frac{\lambda \Delta T}{L^2} \left( \frac{Z_O T_C}{(M_L - 1)(1 + \beta)} \left[ 1 - \frac{\Delta T}{(M_L - 1) T_C} \right] - 1 \right)$$

where;

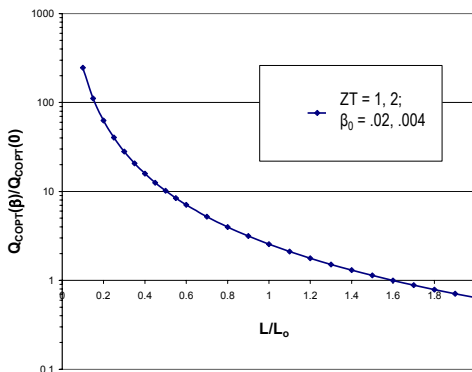
$\lambda$  = TE material average thermal conductivity

AL = Volume of TE material

From equation (16), the amount of material required is inversely proportional to the element length squared. Since  $Z_L$  is a function of  $L$ ,  $COP_{OPT}$  is as well. The minimum value for  $L$  is determined by the amount of decrease in  $COP_{OPT}$  that is acceptable. Figure 4 gives a plot of the percentage change in  $COP_{OPT}$  as a function of  $\beta$  for  $\Delta T/T_C = 0.1$ , and  $Z_O T = 1$  and 2. Figure 5 gives  $Q_{COPT}/AL$  for the same parametric values. All results are the same to the resolution of the graph. By comparing Figures 4 and 5, it can be seen that a knee occurs in the curves so that  $L$  can be reduced to near the break in the curves, defining a minimum value for  $L$  in each case.



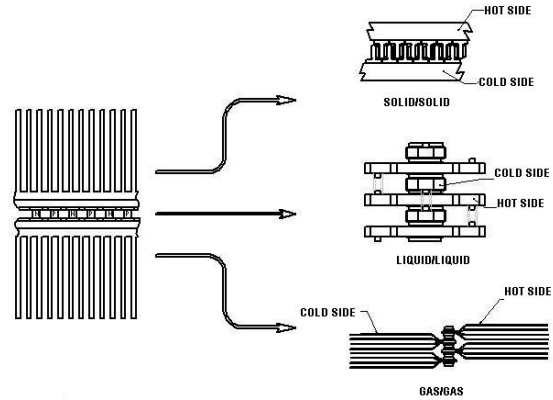
**Figure 4:** System maximum efficiency reduction as a function of  $L/L_0$ .



**Figure 5:** Dependence of  $Q_{COPT}$  on TE element length,  $L$ .

For these calculations, material parameters are assumed fixed, so the total change in  $\beta$  is associated with the length change of the TE element. A practical target value for  $\rho_1$  for the stack geometry is  $\rho_1 = 3 \times 10^{-7} \Omega \cdot \text{cm}^2$ . Using that value, the parameter  $\beta$ , and hence performance, is equivalent to that of the standard geometry when  $L$  is reduced by a factor of about 5, so that material usage can decrease by a factor of about 25.

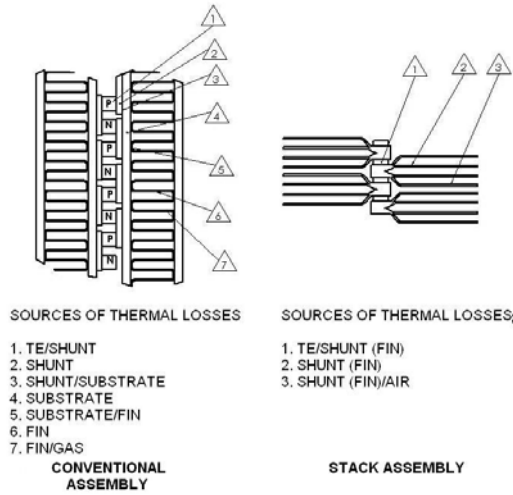
Parasitic thermal losses vary with the geometrical details of a particular configuration. Specifically, optimal power density, and thus, heat flux, is a strong function of the thermal resistance between the source (the TE material/shunt interface) and the output (the heat exchanger interface). As such, three basic configurations exist, depending on whether heat transfer is through solid, liquid or gas interfaces. Since each TE heat pump assembly has two interfaces (both the hot and cold sides) of the types noted, designs should accommodate any combination of these interface types. Figure 6 depicts solid/solid, liquid/liquid and gas/gas stack configurations.



**Figure 6:** Representative stack configurations for solid, liquid and gas interfaces.

Other interface pairings, such as gas/liquid, typically have the corresponding combination of heat exchangers. The different form factors of Figure 6 are required to accommodate the several orders of magnitude differences in diffusivity inherent in the range of interface material types. Solids with high diffusivity can have very small interfaces and thus, small overall dimensions. Liquids are best served by incorporating compact fin structures, with the fins part of both the electrical and the thermal circuits. Such configurations are suitable for liquids that are neither electrically conductive nor corrosive. For other cases, related designs that isolate the thermally and electrically active surfaces are employed. Configurations for gases require heat spreading designs capable of providing large interface areas, such as finned structures, to achieve efficient heat exchange.

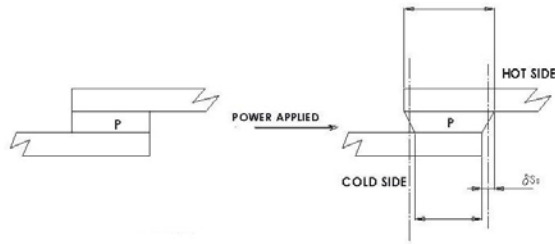
While a more detailed analysis is too dependent on geometrical design and usage to discuss further in general terms, it is useful to compare the relative complexity of the thermal interfaces in a standard device to that of the stack design. Figure 7 identifies the typical interfaces, excluding metal-to-metal interfaces common to both designs (and generally of minor impact on performance).



**Figure 7:** Sources of thermal losses in conventional and stack designs.

In addition to the interfaces in the stack design, the conventional configuration has interfaces associated with the substrate and the separation of the shunt and fin structures necessitated by the inclusion of the substrate. Thus, the stack design can be expected to have, by some computable amount, lower thermal resistance.

In addition to performance reduction, mechanical degradation mechanisms must be taken into consideration when evaluating increased power density designs. While several such mechanisms exist, the major factor for stack designs are associated with thermally induced shear forces within individual TE elements. Figure 8 gives the geometrical parameters that govern such forces caused by differential expansion of the hot and cold side shunts.



**Figure 8:** Shear induced by differential expansion in a stack design TE element.

If both the hot and cold side members expand and contract with the same apparent CTE, coefficient of thermal expansion, the governing equation for a square TE element with a temperature differential of  $\Delta T$  is;

$$(17) \quad \delta S_S = \frac{CTE_S \times W \times \Delta T}{\sqrt{2}\lambda}$$

In a conventional module, the value of the shear,  $\delta_C$ , is governed by the CTE, of the substrate. Ignoring any compliance in solder between the element and shunt and in the bond zone between shunts and the substrate, typical maximum values for  $\delta_{C_{MAX}}$  are;

$$(18) \quad \delta_{C_{MAX}} \approx 1.15 \times 10^{-2}$$

thus, for the stack design, the condition;

$$(19) \quad \frac{CTE_S \times W \times \Delta T}{\sqrt{2}\lambda} \leq 1.15 \times 10^{-2}$$

is imposed. If this condition is satisfied, degradation should be similar to that of the corresponding conventional device.

## Conclusions and Summary

TE system power density in cooling has been shown to be adversely affected by both TE/shunt interface resistance and the shunt resistance. The ratio of these parasitic electrical resistances to TE material resistance are a measure of the degradation in the system level of the figure of merit. Quantitative estimates of the reduction in  $Z_L$  have been expressed in equations (7), and (8), and the resultant decrease in  $COP_{OPT}$ , in equation (13). These losses can be reduced by lowering interfacial resistance and employing stack designs. Crane has modeled such systems for liquids, for a wide range of conditions. His results bear out the ability of the stack configuration to reduce TE material usage. With these changes, TE element length can be reduced by a factor of about 5, compared to a conventional module design, while maintaining the same system-level figure of merit  $Z$ . From equation (16), it is seen that the TE element length change equates to TE material usage reduction of about a factor of 25. Another major source of performance loss is caused by the combined temperature drops across  $\Delta T$  interfaces and within the bulk materials situated between the TE element ends and heat exchange surface. With the stack designs pictured in Figure 6, these losses are usually reduced as shown qualitatively in Figure 7. Quantitative values of performance in terms of  $COP_{OPT}$  as a function of TE material usage can be computed using the simulation tools of Crane [7], or other comprehensive simulation tools.

It is important to recognize that the relationship between the TE and the sum of parasitic electrical resistances,  $\beta$ , is independent of the current applied to the system, and thus, the impact on performance occurs at all power levels in accordance with equations (13) and (16). However, thermal losses are a strong function of heat flux, which is dependent on current, so that such losses degrade performance relatively less at lower currents and power levels. Finally, it is important to note that the very large possible reductions in material usage can lower the contribution of TE materials to overall system cost by such a large factor, that the cost and performance trade-off changes to allow operation at or near  $I_{OPT}$ , and hence, near  $COP_{OPT}$ , rather than closer to maximum cooling power. As a result, operation at maximum efficiency is possible at minimal cost impact in high power output devices, such as HVAC systems for automotive, home and industrial applications. Thus, it becomes possible to seriously consider solid-state HVAC system design based on recent improvements in TE materials, advanced thermodynamic cycles and high power density designs.

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